MEMORY DEVICE WITH NON-VARIABLE WRITE LATENCY

Abstract

One embodiment of the present invention provides a random access memory including a command block and an array of memory cells. The command block is configured to provide a row signal having an active state in response to receiving a write command, wherein the active state occurs at a set time after receipt of the write command, and is configured to provide a write signal having at least a first active state, wherein the first active state of the write signal occurs at a set delay after the active state of the row signal. The array of memory cells is arranged in a plurality of rows and columns, wherein a selected row is opened for access in response to the active state of the row signal, and wherein data is written to at least one memory cell in the opened row in response to the at least first active state of the write signal.